WHAT IS CLAIMED IS:

1. A treatment of a semiconductor device so as to allow substantially completely filled vias, the treatment comprising:

depositing a metal liner layer on a semiconductor device including an aperture;

depositing a seed layer of aluminum on the metal liner layer;

exposing the semiconductor device to a reactive gas; and

depositing aluminum on the seed layer to fill the aperture, whereby the aperture is substantially filled, creating a via.

2. The semiconductor device of claim 1 wherein the via couples a plurality of metal layers through one or more dielectric layers.

3. The treatment of claim 1 wherein depositing a metal liner layer comprises depositing a metal liner layer into the via and onto the surface of a dielectric layer that the via is formed in, the metal liner layer forming a substantially continuous film throughout the topography of the via.

4. The treatment of claim 3 wherein the metal liner layer comprises titanium-based compounds.

5. The treatment of claim 3 wherein the metal liner layer includes titanium nitride.

6. The treatment of claim 3 wherein the metal liner layer comprises titanium.

7. The treatment of claim 1 wherein the depositing a seed layer of aluminum on the metal liner layer comprises depositing a layer of aluminum on the metal liner layer at a temperature such that the seed layer of aluminum does not amalgamate.

8. The treatment of claim 7 wherein the wafer temperature onto which the seed layer of aluminum is deposited is below about 300 degrees centigrade.

9. The treatment of claim 7 wherein the semiconductor device temperature onto which the seed layer of aluminum is deposited is below about 200 degrees centigrade.

10. The treatment of claim 1 wherein exposing the semiconductor device to an atmosphere containing a reactive gas comprises exposing the device to an atmosphere containing a mixture of reactive gasses and inert gasses.

11. The treatment of claim 10 wherein the reactive gas containing atmosphere contains oxygen mixed with inert gasses.

12. The treatment of claim 11 wherein the reactive gas containing atmosphere contains oxygen mixed with argon.

13. The treatment of claim 12 wherein the reactive gas containing atmosphere contains less than about 50% oxygen by weight.

14. The treatment of claim 12 wherein the wherein the reactive gas containing atmosphere contains less than about 10% oxygen by weight.

15. The treatment of claim 10 wherein the reactive gas containing atmosphere is at a pressure of less than about 100mTorr.

16. The treatment of claim 10 wherein the reactive gas containing atmosphere is at a pressure of less than about 10mTorr.

17. The treatment of claim 10 wherein the semiconductor device is exposed to the reactive gas containing atmosphere for a period of time preferably less than about 5 minutes.

18. The treatment of claim 10 wherein the semiconductor device is exposed to the reactive gas containing atmosphere for a period of time most preferably less than about 1 minute.

19. The treatment of claim 1 wherein the wafer temperature onto which the aluminum is deposited is preferably between about 400 degrees centigrade and about 500 degrees centigrade.

20. The treatment of claim 25 wherein the wafer temperature onto which the aluminum is deposited is between about 420 degrees centigrade and about 480 degrees centigrade.

21. A process of fabricating vias and trenches in a semiconductor device, the process comprising:

applying a metal liner layer to a surface and into an aperture of a semiconductor device;

applying a seed layer of aluminum onto the metal liner layer;

treating the semiconductor device with a reactive gas; and

depositing a layer of aluminum onto the seed layer.

22. The semiconductor device of claim 21 wherein the device includes a plurality of metal layers and at least one dielectric layer.

23. The process of claim 21 wherein applying a metal liner layer comprises applying a metal layer onto the surface of the semiconductor device and into the previously formed aperture, the metal liner layer forming a substantially continuous layer over the surfaces of the device and aperture.

24. The process of claim 23 wherein the metal liner layer comprises titanium-containing alloys.

25. The process of claim 21 wherein depositing a seed layer of aluminum on the metal liner layer comprises depositing a layer of aluminum on the metal liner layer such that the seed layer forms a substantially continuous layer throughout the surfaces of the apertures and the semiconductor device.

26. The process of claim 25 wherein the seed layer is deposited at a temperature such that the seed layer of aluminum will not amalgamate.

27. The process of claim 25 wherein the seed layer of aluminum is deposited onto a semiconductor device with temperature below about 300 degrees centigrade.

28. The process of claim 25 wherein the seed layer of aluminum is deposited onto a semiconductor device with temperature below about 200 degrees centigrade.

29. The process of claim 21 wherein treating the semiconductor device with a reactive gas comprises placing the semiconductor device in an atmosphere containing one or more reactive gasses.

30. The process of claim 29 wherein the atmosphere contains oxygen mixed with inert gasses.

31. The process of claim 30 wherein the atmosphere contains oxygen mixed with argon.

32. The process of claim 31 wherein the atmosphere contains less than about 50% oxygen by weight.

33. The process of claim 32 wherein the atmosphere contains less than about 10% oxygen by weight.

34. The process of claim 29 wherein the atmosphere the semiconductor device is exposed to is at a pressure of less than about 100mTorr.

35. The process of claim 29 wherein the atmosphere the semiconductor device is exposed to is at a pressure of less than about 10mTorr.

36. The process of claim 29 wherein the length of exposure of the semiconductor device to the atmospheres is less than about 5 minutes.

37. The process of claim 29 wherein the length of exposure of the semiconductor device to the atmospheres is less than about 1 minute.

38. The process of claim 21 wherein the temperature of the semiconductor device at the time of aluminum deposition is between about 400 degrees centigrade and about 500 degrees centigrade.

39. The process of claim 21 wherein the temperature of the semiconductor device at the time of aluminum deposition is between about 420 degrees centigrade and about 480 degrees centigrade.

40. A process of forming vias and trenches on a semiconductor device that allows for:

vias and trenches with width of less than about .18$\mu$m and with an aspect ratio of greater than about 6:1 to be substantially filled; and

substantial filling of large vias and trenches.